

**BASE PAD LAYOUT FOR REDUCING PARASITIC BASE-COLLECTOR
CAPACITANCE AND METHOD OF FABRICATING HBT USING THE
SAME**

5 BACKGROUND OF THE INVENTION

The present invention relates to a base pad layout for reducing the parasitic base-collector capacitance and method of fabricating HBT using the
10 same. More particularly, the invention relates to a Heterojunction Bipolar Transistor fabricating (HBT) method where the base-collector capacitance due to base pad could be reduced through a simple base pad layout that utilizes the fabricating method of a
15 triple mesa heterojunction bipolar transistor using wet etching which isolates an active base region and a base pad region.

Currently, a worldwide active research work is being undertaken in the area of ultra-high speed wide-
20 band cable and wireless communication in order to meet an explosive increase in Internet users and a rapid shift towards a high capacity data transmission for moving image files from a low capacity data transmission for simple pictures or text files.

25 Some of the ultra-high speed wide-band communication networks include Local Multipoint Distribution Services (LMDS) (28 GHz band) for

wireless communication and optical fiber communication
(OC-768 (40Gbps optical fiber network))

In order to meet the rapid increase in
information services, more bandwidth should be
5 available in the future. At the present, active
research on the ultra-high speed wide-band
communication networks for a bandwidth over 100Ghz is
being carried out.

Most of all, the miniaturization, performance
10 improvement and development of semiconductor devices
that function in the high frequency band are very
important in order to construct ultra-high speed wide-
band communication networks.

Accordingly, high-speed performance semiconductor
15 devices are actively being researched.

Especially, a heterojunction bipolar transistor
is attracting a lot of attention as an ultra high
frequency semiconductor device that can be used to
transmit/receive data in an ultra high-speed
20 communication network. Active research is being
concentrated on reducing the parasitic component of
the device for a better ultra high-speed performance.

It has been discovered that the ultra high-speed
performance of HBT is constraint by the base-collector
25 capacitance. To date, many research works on reducing
the base-collector capacitance for an ultra high-speed
performance have been published.

The maximum oscillation frequency f_{\max} can be approximated by base resistance R_B , base collector capacitance C_{BC} and current gain cutoff frequency f_T as shown in Equation 1

5

[Equation 1]

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$$

10 As can be seen from Equation 1, the performance speed of HBT increases with a decrease in the base-collector capacitance.

The above base-collector capacitance can largely be separated into the capacitance due to an active
15 base region and the capacitance due to a base pad for interconnect via.

With the improvement in the device fabrication technology recently, the active base region is being scaled down proportionately with the scale down of the
20 active region. However, the scale down of the base pad is harder to achieve due to the complexity of the via process.

Accordingly, the recent technology allows an almost equal size for both base region and base pad
25 region.

More specifically, in accordance with the scale down of the devices, the size of the parasitic

capacitances for both base region and base pad region are almost equal. For the perspective of reducing the base-collector capacitance, it is of paramount importance to reduce the capacitance in the base pad
5 region.

U.S. Pat. Nos. 4,380,774 (Title: High performance bipolar microwave transistor) and 5,672,522 (Title: Method of making selective sub-collector heterojunction bipolar transistor) both disclose
10 methods for reducing the base-collector capacitance using the base pad of HBT.

These prior arts rely on ion implantation and epitaxy re-growth methods for reducing the base-collector capacitance. However, these methods require
15 costly equipment such as ion implantation apparatus and also involves an epitaxy re-growth process that is associated with the reliability and repeatability problems.

Hyunchol Shin, Gaessler C., and Leier H. disclose
20 other prior arts on double polyimide planarization process, titled as "Reduction of base-collector capacitance in InP/InGaAs HBT's using a novel double polyimide planarization process", in IEEE Electron Device Letters (Volume 14, Issue 8, pp 297-299,
25 August 1998). However, the fabrication process disclosed in the paper is very complicated and the process involves a reactive ion etching that could

damage the HBT device.

SUMMARY OF THE INVENTION

5 The present invention is designed to overcome the above problems of prior art. The object of the present invention is to provide a Heterojunction Bipolar Transistor fabricating (HBT) method where the base-collector capacitance due to base pad could be reduced
10 through a simple base pad layout that utilizes the fabricating method of a triple mesa heterojunction bipolar transistor using wet etching which isolates an active base region and a base pad region.

 According to the present invention, the base pad
15 layout for reducing the parasitic base-collector capacitance comprises a base region aligned in a $\langle 011 \rangle$ or $\langle 0\bar{1}1 \rangle$ orientation with respect to the semiconductor substrate and a base feeding region which connects the base region and the base pad region.

20 The method for fabricating a triple mesa HBT using the base pad layout according to the present invention comprises the processing steps of: a first process for isolating a base region and a base pad region and forming a base pad layout by connecting
25 said regions to a base feeding region; a second process for sequentially stacking a sub-collector InGaAs layer/an etching stopper InP layer/ a base-

collector InGaAs layer/an emitter InP layer/ an
emitter cap InGaAs layer on a semi-insulating InP
substrate using the epitaxy growth method; a third
process for depositing a base metal using said base
5 pad layout as a mask after depositing a emitter metal
on the epitaxy structure formed in said second process
and sequentially etching the emitter cap InGaAs layer
and the emitter InP layer to allow said emitter metal
to self-align and to expose the upper side of the
10 base-collector InGaAs layer; a fourth process for
defining a first photoresist to some parts of the base
region and the base feeding region in order to protect
an emitter region; a fifth process for forming a void
area underneath the base feeding region using side
15 etching after exposing the upper side of the sub-
collector InGaAs layer by etching the base-collector
InGaAs layer and the etching stopper InP layer using
said first photoresist and base metal layer as a mask;
a sixth process for depositing a collector metal on
20 said sub-collector InGaAs layer; and a seventh process
for defining a second photoresist in order to protect
the lower part of the emitter and the base region and
removing said second photoresist after isolating the
base region and the base pad region by side etching
25 the sub-collector InGaAs layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a plan view of the base pad layout according to the present invention where FIG. 1a shows a $\langle 01\bar{1} \rangle$ orientation and FIG. 1b shows a $\langle 011 \rangle$ orientation.
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FIG. 2 shows a standard epitaxy structure for the HBT device that is required by the present invention.

FIG. 3a through 3f show cross section diagrams of the HBT device according to the fabrication process of
10 the present invention.

FIG. 4 shows a structural diagram of the HBT device fabricated according to the fabrication process of the present invention.

FIG. 5 shows an electro-microscopic picture of
15 the HBT device fabricated according to the fabrication process of the present invention.

<Description of the numeric on the main parts of the drawings>

111: Semi-Insulating InP Substrate
20 112: Emitter Cap InGaAs Layer
113: Emitter InP Layer
114: Base-Collector InGaAs Layer
115: Etching Stopper InP Layer
116: Sub-Collector InGaAs Layer
25 121: Emitter Metal Layer
122: Base Metal Layer
122a: Base Pad Region

122b: Base Feeding Region
122c: Base Region
123: Collector Metal Layer
131, 132: Photoresist

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DETAILED DESCRIPTION OF THE EMBODIMENTS

Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

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The methods disclosed in the present invention could both be implemented to a single HBT and double HBT. The preferred embodiments hereafter will be described with reference to the single HBT.

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FIG. 1 shows a base pad layout as a mask layout for depositing the base metal layer 122 in FIG. 3a.

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The base pad layout comprises a base region 122c aligned in a $\langle 01\bar{1} \rangle$ or $\langle 011 \rangle$ orientation on the substrate; a base pad region 122a aligned in a rectangular shape (square or rectangular) which is sloped (45 degree) against said base region 122c and a base feeding region 122b aligned in a $\langle 010 \rangle$ orientation and connects said base region 122c and said base pad region 122a.

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The main feature of the present invention is isolating the base region 122c and the base pad region 122a and forming a base pad layout by connecting the

regions to the base feeding region 122b. This differentiates the present invention with other methods that define a base pad region on an extended part of the conventional base region.

5 Above all, this structure as shown in FIG. 3 is for forming a void area between the base pad region 122a and the base region 122c by side etching underneath the base feeding region 122b.

10 This base pad layout is based on the facts that the etching speed is faster in $\langle 010 \rangle$ direction than $\langle 01\bar{1} \rangle$ or $\langle 011 \rangle$ direction and almost no etching occurs in $\langle 011 \rangle$ direction when wet etching the InP layer.

15 Utilizing the above layout, all epitaxy structures except the semi-insulating InP substrate 111 can be etched to reduce the base-collector capacitance for the lower part of the base feeding region 122b as shown in FIG. 3e.

20 By isolating the base region 122c and the base pad region 122a, the parasitic capacitance could be electrically isolated from the HBT's base-collector capacitance.

25 The InP layer and InGaAs layer underneath the base pad region 122a simply act as a post which supports the base pad region 122a without having any electrical role. As a result, the base-collector capacitance due to the base pad is significantly reduced.

FIG. 2 shows a standard epitaxy structure for InP/InGaAs SHBT or DHBT that is required by the present invention.

Using the epitaxy growth methods such as MetalOrganic Chemical Vapour Deposition MOCVD or Molecular Beam Epitaxy (MBE), an sub-collector InGaAs layer 116/an etching stopper InP layer 115/ a base-collector InGaAs layer 114/an emitter InP layer 113/ an emitter cap InGaAs layer 112 are sequentially stacked on a semi-insulating InP substrate 111.

FIGS. 3a through 3f show cross section diagrams of the HBT devices which are fabricated according to the present invention.

The fabrication method of the HBT devices according to the present invention which comprises the step of depositing an emitter metal layer 121 which aligned in a $\langle 01\bar{1} \rangle$ or $\langle 011 \rangle$ orientation in FIG. 3 on the epitaxy structure as shown in FIG.2; sequentially etching the emitter cap InGaAs layer 112 and the emitter InP layer 113 to allow the base metal layer to self-align; and depositing the base metal layer 122 on the upper part of the base-collector InGaAs layer 114 using the base pad layout 112a, 122b, 122c as a mask.

Afterwards, a photoresist pattern 131 for protecting the emitter region as shown in FIG. 3b is defined on some parts of base feeding region 133 and based region 122c.

Afterwards, the base-collector InGaAs layer 114 and the etching stopper InP layer 115 are sequentially etched using the photoresist pattern 113 and base metal layer 122 as an etching mask.

5 In this process, the base pad region and base region are isolated by side etching underneath the base feeding region using the anisotropic etching characteristic where the etching speed varies according to the crystal lattice direction.

10 In this case, the etchant used is H₃PO₄: H₂O₂: H₂O as in the case of etching base-collector InGaAs layer 114.

Due to a high selectivity value between the etching stopper InP layer 115 and the base-collector
15 InGaAs layer 114 for the etchant H₃PO₄: H₂O₂: H₂O, almost no etching occurs for the etching stopper InP layer 115.

Also, due to a high selectivity value between the etching stopper InP layer 115 and the sub-collector
20 InGaAs layer 116 for the etchant HCl: H₃PO₄, almost no etching occurs for the sub-collector InGaAs layer 116.

In another words, the sub-collector InGaAs layer 116 and the etching stopper InP layer 115 could selectively be etched using the above etchant and
25 small amount of over etching does not cause a serious problem.

In the above process, since the lower part of

base feeding region (the void area underneath the left base metal layer 122 in FIG. 3c) is aligned in $\langle 010 \rangle$ direction, a fast side etching occurs resulting a void area.

5 In this instance, the etching speed is dependent upon the type of etchant, concentration and temperature.

 Afterwards, a collector metal layer is deposited on the sub-collector InGaAs layer 116 as shown in FIG.
10 3d.

 Afterwards, a photoresist pattern 132 is defined on the whole area except the base pad region 122a for protection and the sub-collector InGaAs layer 116 is etched as shown in FIG. 3e.

15 In this process, the base pad region and base region are isolated by side etching underneath the base feeding region using the anisotropic etching characteristic where the etching speed varies according to the crystal lattice direction.

20 In this case, the etchant used is H_3PO_4 : H_2O_2 : H_2O as in the case of etching base-collector InGaAs layer 114.

 Due to a high selectivity value between the etching stopper InP layer 115 and the semi-insulating
25 InP substrate 111 for the etchant H_3PO_4 : H_2O_2 : H_2O , almost no etching occurs for the etching stopper InP layer 115.

In this instance, the etching speed is dependent upon the type of etchant, concentration and temperature.

In the above process, the base-collector capacitance could be reduced by etching the whole of the lower part of the base feeding region 122b (where a void area is formed) except the semi-insulating InP substrate 111.

Also, by isolating the base region and the base pad region, the parasitic capacitance could be electrically isolated.

The InP layer and InGaAs layer underneath the base pad region simply act as a post which supports the base pad region without having any electrical role. As a result, the base-collector capacitance due to the base pad is significantly reduced.

Finally, the final HBT structure is completed by removing the photoresist pattern 132 as shown in FIG. 3f.

The base-collector InGaAs layer 114 which is used for a base collector layer for the single HBT could be a base layer for the double HBT. The InP layer 115 which is used for an etching stopper layer for the single HBT could be a collector layer for the double HBT.

FIG. 4 shows the final HBT structure after undergoing the processes in FIG. 2 and FIG. 3a through 3f.

FIG. 5 shows an electro-microscopic structure after undergoing the processes in FIG. 2 and FIG. 3a through 3d.

FIG. 4 and FIG. 5 show the final results of the
5 present invention.

As disclosed so far in the present invention, the base-collector capacitance due to base pad could be reduced through a simple base pad layout and wet etching which isolates an active base region and a
10 base pad region.

Since the present invention uses the conventional wet etching method for fabricating a triple mesa HBT involving only a small modification of the base pad layout, no additional process is required.

15 The present invention provides a simple base pad layout that utilizes wet etching which isolates an active base region and a base pad region in order to reduce the base-collector capacitance from the base pad.

20 According to the present invention, the new base pad layout in the HBT device fabrication process uses the conventional process without the need for additional processes and brings about an economic advantage of reducing the time required for
25 technological development.

Also, the new base pad layout could be applied not only to InP/InGaAs but also various types of

compound semiconductors that use the mesa structure including Heterojunction Field Effect Transistor (HFET), Photo Diode, Photo Transistor.